WE CLAIM:

1. An integrated semiconductor circuit, comprising:

plurality of memory cells each memory cell having a selection transistor and a storage capacitor, each memeory cell being driven electrically by bit lines and word lines; and

a plurality of electrical contact structures being arranged at the level of the word lines, the contact structures electrically connecting the bit lines to the selection transistors of the memory cells the contact structures leading past the word lines and being insulated from the word lines by lateral insulations, and in each case two, mutually adjacent bit lines being connected to a common signal amplifier,

wherein additional contact structures are provided, the additional contact structures leading past the word lines, the additional contact structures representing dummy contacts, in which case, for each contact structure which proceeds from a bit line leads past a word line, and connects the bit line to a memory cell, a dummy contact, which proceeds from the adjacent bit line connected to the signal amplifier and leads past the same word line as the respective contact structure is provided

2. The semiconductor circuit as claimed in claim 1, wherein the contact structures, which connect a bit line to a memory cell, and the contact structures, which represent dummy contacts, lead past alternately along a word line.

3. The semiconductor circuit as claimed in claim 1, wherein

the storage capacitors are trench capacitors arranged in a semiconductor substrate, and the bit lines are arranged on the semiconductor substrate at a greater distance from the semiconductor substrate than the word lines.

4. The semiconductor circuit as claimed in one of claim 1, wherein the dummy contacts in each case end above a trench isolation, whereas the remaining contact structures in each case lead into a common doping region of two selection transistors.

5. The semiconductor circuit as claimed in claim 1, wherein the selection transistors are field-effect transistors, the gate electrodes of which are formed by the word lines.

6. The semiconductor circuit as claimed in claim 1,wherein the lateral insulations between the contact structures and the word lines are sidewall coverings of patterned gate layer stacks.

7. The semiconductor circuit as claimed in claim 1, wherein the semiconductor circuit is a dynamic random access memory.